ABSTRACT OF THE DISCLOSURE

To reduce the amount of data that should be stored on a memory-built-in timing generator for generating timing pulses for use to drive a solid-state imaging device, V- and H-counters, three ROMs, V- and H-comparators and combinatorial logic circuit are provided. The V- and H-counters perform a count operation responsive to vertical and horizontal sync signal pulses as respective triggers. One of the ROMs stores time-series data representing a logical level repetitive pattern of an output pulse train. The other two ROMs store edge data representing at what counts of the V- and H-counters control pulses should change their logical levels. The V- and H-comparators and the combinatorial logic circuit change the logical levels of the control pulses when the counts of the V- and H-counters match the edge data. The comparators and logic circuit also output, as the timing pulses, results of logical operations performed on the output pulse train, represented by the time-series data, and the control pulses.